The first and second compositions utilized in the above embodiments may be the same or different.

The above steps may be carried out employing any of the embodiments described hereinabove, as well as others. For example, the component on the wafer, preferably the polymeric material, may be deposited using a chemical vapor deposition (CVD) method. CVD methods are known in the art, and one example of a CVD method is described in U.S. Patent No. 6,045,877 to Gleason et al. A particularly preferred polymeric material is a fluoropolymer.

The fluid composition may comprise various materials such as, in one embodiment, carbon dioxide or a carbon dioxide/co-solvent mixture.

The present invention may be carried out by employing various processing equipment. In one embodiment, for example, a spin coater can be used to deposit polymeric material on the substrate. One example of a spin coater is described in U.S. Patent No. 6,001,418 to DeSimone et al. that has ports, sub-chambers, to accommodate imaging, CO_2 removal, vacuum development, and/or stripping techniques. This embodiment provides one example of an IMPD. Modifications from the above may be made without departing from the scope of the invention.

The present invention is highly advantageous in that the deposition, development, and removal (e.g., stripping) of the resist used in processing microelectric substrates can be carried out in a closed system, in contrast to conventional solvent-based processes. Moreover, due to the environmentally benign nature of carbon dioxide, and CO_2 mixtures mentioned herein, and its relative ease of handling, one has the ability to design microelectronics processing equipment (e.g., metal deposition facilities, etch processes, and O_2-Reactive Ion Etch (RIE) processes that are integrated with carbon dioxide based deposition, development, and stripping equipment. Moreover, post-processed carbon dioxide is typically easier to recover than organic or aqueous wastes. The low solvent viscosity of carbon dioxide and CO_2 solutions also makes it highly desirable for penetrating increasingly smaller gaps between features in microelectronic substrates. Such an integrated

design of the microelectronics processing equipment can avoid the repeated entry, removal, and re-entry steps that are believed to be inherent in non-integrated processes. In one embodiment, for example, one could process a wafer repeatedly within one device without removing it in order to spin coat or develop a photoresist coating. Such an integrated system can therefore eliminate or significantly reduce the need for extensive and costly clean room facilities that are often required to reduce wafer contamination upon removal from closed systems.

In other embodiments, the processes of the invention may include other steps. For example, in embodiments where an intermediate layer is present between the coating portion and the substrate, the process may further comprise the step of selectively etching the intermediate layer using the developed coating portion as an etching mask. The intermediate layer may comprise many of the components set forth herein, the selection of which is known to one skilled in the art. In a preferred embodiment, the intermediate layer is present in the form of a planarization layer such as one comprising a novalac resin, or an interlayer dielectric resin such as one selected from the SiLK™ family of dielectric resins made commercially available from The Dow Chemical Company located in Midland, Michigan. Exemplary resins in the SiLK™ family include SiLK™ I Resin SiLK™ H Resin, and CYCLOTENE™* Resins

The etching may be carried out by employing various techniques known to one skilled in the art. For example, the step of selectively etching the intermediate layer comprises contacting the intermediate layer with a gas selected from the group consisting of oxygen, chlorine, fluorine, and mixtures thereof. It should be appreciated that the term "etching" is broadly defined and may include methods which completely or partially expose the underlying substrate. The etching step may be used in conjunction with any of the other steps described herein as deemed appropriate by one skilled in the art. For example, subsequent to etching, the exposed substrate may be contacted (e.g., showered) with metal-containing materials doped with an ionic material

including inorganic ions such as, without limitation, boron, arsenic, or phosphorous.

The present invention will now be described by the examples which follow. It should be understood that these examples merely illustrate the invention, and do not limit the scope of the invention as defined by the claims.